resist, the nitride, GeO_2 and pad oxide are etched selectively to fill 410 to the original silicon wafer surface 620 to form the pillar mold 610, as shown in Figures 6A - 6C, and the resist stripped. The silicon pillar 710 is then epitaxially and selectively grown from the original silicon wafer surface 620 to fill the mold 610 and the surface planarized to result in the structure shown in Figures 7A - 7C. If pattern 520 is of sub-lithographic width, as can be achieved by, for example, a phase shift mask, the pillar/conduction channel will be of corresponding sub-lithographic dimensions.

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Then, as shown in Figures 14A - 14C, a sacrificial oxide 1430 is formed on exposed silicon surfaces and stripped. The gate dielectric 1420 is formed self-aligned with the channel by either oxidation or CVD, atomic layer epitaxy or the like that may completely surround the channel. At this point, a heat treatment can be performed to move the out-diffused dopant regions 1410 from the ASG and BSG to form the drain in the lower part of the transistor. This out-diffusion must eventually reach the implanted regions 160, 170, respectively. The trench 1430 is then filled with a gate material (self-aligned with the channel and gate dielectric) such as polysilicon to create gate electrodes 1440 (Figure 15A - 15C) that are initially joined forming an interior wall completely surrounding the channel but which can be later separated by polishing gate 1440 and residual dopant films such as 1440 that are still present down to nitride 910, recessing the gate material at 1510, and depositing nitride 1550 in the recess, as shown in Figure 15A - 15C. Then the gate material is further recessed at 1510 and TEOS is deposited and then etched to form sidewall spacers 1520.